A Low Noise Figure 1.2-V CMOS GPS Receiver 
Integrated as a Part of a Multimode Receiver

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Abstract—This paper presents the designed and measured performance of a Global Positioning System (GPS) receiver chain integrated as a part of a multi-band and multimode receiver, designed for global system for mobile communications (GSM) and wideband code division multiple access (WCDMA). Adding an additional mode to a receiver with minor changes to the implementation is discussed. The IC is implemented in a 0.13-µm CMOS technology without any analog options. At 1.2-V supply voltage and total power dissipation of 49 mW for the analog signal path, the proposed GPS receiver features a noise figure of 2.2 dB.

I. INTRODUCTION
There is an increasing demand for mobile devices supporting several wireless communication systems in the mobile communication market [1]. This also sets pressure for lower power, higher integration and lower cost for the radio implementation, and moreover for combining requirements of several standards to single RF ASIC specification [2]. Recent CMOS implementations show the capability to single-chip radio integration [3],[4], and high performance at low supply voltages [5]. Also multiple radio systems can share the hardware if interworking schemes allow it [6]. The motivation to combine wideband code division multiple access (WCDMA) and global system for mobile communications (GSM) signal path with Global Positioning System (GPS) can come from two issues. First, the GPS can be combined with diversity branch if such is used in the reception, and second the modifications in ASIC design may be so minor that it is more efficient way of developing the solution.

In this paper we both increase the level of RF integration combining analog and digital circuitry on the same ASIC and combine the requirements of several radio standards in the same signal processing paths i.e. receiver chains. We describe how a GPS mode [7] can be added to a receiver supporting GSM and WCDMA systems, with only minor additions and changes to the circuitry. As a result, the GPS receiver demonstrates the state-of-the-art performance with low power consumption. This paper is structured so that the system requirements and architecture of a GPS receiver is presented in Section II. In Section III, the needed changes to the different building blocks are presented. Measured performance and conclusions follow in Sections IV and V, respectively.

II. GPS RECEIVER

A. System Requirements
The GPS system differs from the cellular systems in many ways. In GPS we only need to support one channel of reception. It has no adjacent channels to be filtered and no hard linearity and blocker requirements from the system point of view. A wide enough channel width ensures the reception of additional side lobes, which reduces the needed acquisition time in GPS reception. The received signal can be quite small and a good sensitivity is needed, setting a low noise figure (NF) requirement, which results in a reasonable high gain requirement for the receiver compared to GSM and WCDMA modes. The GPS L1 band of choice (1575.42 MHz) is in the middle of the high and low cellular bands.

The GPS system requirements get immediately harder when it needs to work in a mobile terminal environment. GPS system specification has internally no hard linearity and blocker requirements but looking at the operation environment, a mobile phone application poses a set of additional requirements to the receiver. In a mobile device there maybe quite many other radios operating simultaneously. The intermodulation distortion products of those can be quite harmful for the GPS reception. Adding additional filtering between the antenna and RF IC is not wanted. An additional band filter would cause, with the added losses, undesired increase in the noise figure. So an additional low-noise amplifier (LNA) would then be needed.
for complying to the noise figure requirement, which again reduces the receiver linearity with the added gain. Final solution would be very expensive and bulky. A better way is to have good enough off-band linearity in the fully integrated receiver.

B. Receiver Architecture

The direct conversion receiver architecture has been chosen for the high integration possibilities. The direct conversion receiver is also suitable for integrating different systems because no complex frequency planning is needed and the building blocks are relative easy to be made suitable for supporting different modes and therefore can be reused for gaining die area and design work. All systems set different requirements for the receiver, such as gain, noise figure, linearity and adjacent channel selectivity. Need of supporting system specific requirements combined to wide band operation sets naturally very demanding building block specification compared to only supporting single band and mode. In a CMOS direct conversion receiver the biggest challenge is to have a low 1/f noise in GSM and high linearity inside the system in WCDMA. The GPS mode sets stringent requirements for the noise, as also for the off-band linearity. Typical requirements for noise and linearity referred to LNA input are given in Table I. The most challenging off-band linearity cases for GPS were found to be the intermodulation distortion product of Bluetooth & GSM850.

III. RECEIVER BUILDING BLOCKS

The building blocks were designed taken GSM and WCDMA requirements into account. The multi-band requirements are also considered in the designing of some of the blocks where the added frequency range is needed even if perhaps not every block supports every band in this implementation. The aim is to reuse the building blocks as much as possible between systems and bands. The reuse restricts the receiver to only be operational at one system at a time. The receiver architecture is shown in Fig. 1.

A. LNA

Frequency specific antennas and band specific system filters set the requirement for own inputs in the LNA for each frequency band. The reason for this is that switches in the signal path are unwanted especially in GPS, because of the added loss and nonlinearity. Therefore separate input stages are combined after cascode devices. The LNA structure is shown in Fig. 2. The load resonators consist of tunable LC-tanks. Because the major interference and blocker signals are out-of-band signals, some additional filtering can be achieved by having high Q values in the matching and load resonator. This is the reason why the GPS LNA signal path is completely separate from the other bands. There is a capacitor matrix in the resonator for adjusting the process variation, which is an inherent issue with high Q resonators.

<table>
<thead>
<tr>
<th>SYSTEM</th>
<th>GSM</th>
<th>WCDMA</th>
<th>GPS</th>
</tr>
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<tbody>
<tr>
<td>NF</td>
<td>3</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IIP3</td>
<td>-19</td>
<td>-10</td>
<td>-</td>
</tr>
<tr>
<td>IMD3 (PCS &amp; 802.11a)</td>
<td>-</td>
<td>-</td>
<td>-120 dBm</td>
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<tr>
<td>IMD2 (Bluetooth &amp; GSM850)</td>
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<td>-120 dBm</td>
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B. Downconversion Mixer

The downconversion mixer is common for all modes and bands. It consists of separate input stages, which are combined to the switching core transistors resulting in combined outputs for the analog baseband circuit, shown in Fig. 3. Two low area differential coils are needed in the mixers for achieving low flicker noise for GSM [3], [9]. The mixer resonator has a capacitor matrix for tuning slightly the center frequency for the GPS frequency band. This resonator helps also in off-band linearity cases.

Figure 1. Block diagram of the receiver

Figure 2. Schematics of the LNA
The analog baseband circuit, shown in Fig. 4., could use the same approach as given in [10]. The circuit is a 2nd order Chebyshev active-RC low-pass filter with an additional passive pole in the front of the filter. The gain adjustment is made by adjusting the input resistors (RINN, RINP) while the nominal gains for the different modes is set with the filter resistors (R1-R3). Filter bandwidth selection and process variation tuning of the corner frequency is controlled with the tunable integrator capacitors (C1-C2). The capacitor matrix is the same for all modes. The wideband mode for GPS was added to the design simply by dividing the WCDMA capacitors by two. Additional gain adjustment was done by adding more control range into the input resistors.

D. ADC and Digital Frond-end

The analog-to-digital converter (ADC) is based on a \( \Sigma \Delta \)-modulator topology [11], [12]. The structure of the modulator is a 1-bit, 2-2 cascade topology. Mode selection is made by selecting suitable sampling clock modes. The GPS could use directly the WCDMA mode, which has the highest sampling rate of 153.6MS/s. The dynamic range will decrease in the wide bandwidth GPS mode compared to WCDMA because of the noise shaping in the \( \Sigma \Delta \)-modulator. This is not a problem in GPS because there are no adjacent channel selectivity requirements and the limited dynamic range is handled by appropriate gain adjustments.

The digital frond-end consists of final filtering and scaling in the digital domain. These functions can easily be programmable to different modes.

E. Synthesizer

The different modes and bands set hard requirement on the voltage-controlled oscillator (VCO) and phase-locked loop (PLL). It is a demanding task to design only one single VCO complying for all different phase noise requirements over the large frequency range. In the receiver the frequency generation is divided between two VCO’s taken also the low-band cellular system requirements into account. The receiver uses a divide-by-2 and a divide-by-4 for getting the right local oscillator signals to the downconversion mixers. The GPS phase noise requirements are not demanding, the only challenge is getting the right frequency generated. The divide-by-2 is used for generating the GPS LO.

In the receiver a fractional PLL is employed, which can easily be used for generating the wanted frequency from any available reference frequency.

IV. Experimental Results

The circuit was fabricated using a 0.13-µm CMOS process, using a 1.2-V power supply and no analog process options. It was mounted to a ball-grid-array (BGA) package and measured with an off-chip surface-mounted-device (SMD) balun. The off-chip balun used in the measurements has a typical loss of 0.7dB. The loss has been de-embedded from the results.

The measured performance of the GPS is summarized in Table II. The results presented here are from an analog measurement of the complete receiver from LNA input to analog baseband outputs. Implemented ASIC is shown in Fig. 5. and the measured spectrum of the GPS receiver after digital filtering in Fig. 6. The total area of the presented blocks is 6.6 mm\(^2\).
Figure 6. CW signal measured from digital filter outputs

TABLE II. GPS RECEIVER MEASURED RESULTS

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<table>
<thead>
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<tr>
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<td>dB</td>
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<tr>
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<td>IMD2 (Bluetooth &amp; GSM850)</td>
<td>-122.5</td>
<td>dBm</td>
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</table>

One of the most important characteristics of a GPS receiver in a mobile terminal is how good the off-band linearity is. One band filter is assumed to be utilized in front of the RF IC part of the receiver for attenuating a large portion of the interference signals. The third-order intermodulation distortion is measured using two continuous wave (CW) signals, one representing a PCS signal with leaked power of -35 dBm and the second representing an 802.11a signal having a power of -22 dBm. The IMD3 component was measured to be -141.5 dBm, which is low enough for not disturbing the GPS reception. The second-order intermodulation signal was measured to be -122.5 dBm, which also is low enough not to deteriorate the reception.

V. CONCLUSIONS

We have presented an implementation having necessary changes for adding a GPS mode to a multimode CMOS receiver. The changes and additional circuitry are relatively small. The biggest changes are applied to the RF part of the circuitry for having wide enough bandwidth in the VCO and dedicated inputs in the LNA. The design of a CMOS multimode and multi-band receiver requires more attention in architectural and system design. Extra effort is required on the receiver building blocks for complying with the different requirements from all systems. With careful design the receiver can reach a state-of-the-art performance with low power consumption. We demonstrated a GPS receiver designed for the hostile environment in a mobile device having a very low NF of 2.2 dB and good off-band linearity for being immune for the most severe interference signals in a mobile terminal.

ACKNOWLEDGEMENT

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