A GaN HEMT Amplifier with 6-W Output Power and >85% Power-Added Efficiency

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The 2007 IEEE MTT-S student power amplifier competition requires students to design and fabricate a highly efficient power amplifier. Recently published results show power amplifiers in the low GHz range with efficiencies greater than 80% [1], [2]. This article presents the winning power amplifier implemented with a gallium nitride (GaN) high electron mobility transistor (HEMT) and having power-added efficiency (PAE) greater than 85%. It will be shown that computer-aided design (CAD) simulation tools, accurate device models, and sensible design rules can produce first-pass power amplifier design success. An overview of design, fabrication, and testing processes is presented here together with measured results.

Design
The aim of the competition was to design a power amplifier with the highest efficiency at an output power above 5 W and at a frequency above 1 GHz. To meet these criteria this amplifier was designed for an output frequency of 1.2 GHz, an output power of >38 dBm, and an efficiency above 80% (last year’s winner!).

The transistor chosen for this design was a 10-W RF power GaN HEMT from Cree (CGH40010). Venkata Gutta, a colleague at Macquarie University, suggested the device and the samples were easily obtained, courtesy of Cree. The transistor used is available in a screw-down package and is not internally matched. It comes with an accurate nonlinear model, which is critical for the design of high-efficiency power amplifiers.

Applied Wave Research’s (AWR’s) Microwave Office software was used for the design of the amplifier. It is an integrated environment that allows the design and simulation of printed circuit board or integrated circuit RF circuits as well as providing seamless connection to electromagnetic (EM) simulators such as Sonnet.

Designing and building an amplifier is a refreshing change from integrated circuit design as the amplifier can be tweaked, transmission lines can be modified if needed, and it can be held firmly in two hands!

The design and modeling strategies employed are similar to that presented in [3] but were adapted to deal with a nonlinear amplifier rather than Class A. Instead of using multimeter software to synthesize the input and output matching networks, an input and load termination optimization method was used to obtain the maximum PAE, and matching networks were designed around these components.

At the heart of any efficient amplifier is a switch. The switching action results in output currents or voltages that resemble a square wave. While the PAE calculation is concerned with power at the fundamental (and, hence, harmonics should be minimized), these harmonics need to be present or otherwise the current and voltage waves cannot exist in any other form than a pure sinusoid. Due to this, impedances at all harmonics up to the fifth were included in the input and output matching tuners.
At this stage, it needs to be pointed out that this amplifier was designed without a class. The main concern was what harmonic impedances could be provided at the input and output of the amplifier in order to obtain maximum efficiency.

To model the effect of different terminations at the input and output of the transistor, an optimization routine was set up where the impedance (magnitude and phase) presented to the input and output for five harmonics was a parameter as well as the bias and drain voltage. Loose convergence tolerances were set in the harmonic balance simulator and the goals of the optimization were set to >85% PAE with >6 W of output power at 1.2 GHz.

The efficiency generated by this method was 88% at 1.2 GHz with an output power just above 6 W.

The next step is to take the ideal components (impedance tuners) at the input and output of the transistor and turn them into real matching networks made up of transmission lines and capacitors. The transistors are bilateral in this configuration, so a change of output impedance affects the input impedance and vice versa. One of the advantages of using this method allows the input match to be designed with the output matched in a condition that achieves high efficiency (i.e., with the lossless matching network). This reduces the amount of time re-optimizing the input match as the output match is changed.

As time was limited, a trial-and-error approach was used to transform the ideal impedance tuners into real matching networks. In the future, an automated method that takes the parameters from the source and load tuners and creates the matching networks could be employed.

The resulting input matching networks are shown in Figure 1.

Figure 1. Simplified schematic for the power amplifier showing input and output matching networks.

Figure 2. EM networks for the input and output analyzed using Sonnet.
shortened by approximately 5 mm at each port and a transmission line component was used. This allowed Sonnet to take care of any step and coupling effects, and the variable transmission lines in the schematic are used to tune out any differences. Only one EM simulation was needed for each network, taking a few minutes to simulate and providing a more accurate model.

Inspiration for the layout was taken from the Cree reference designs, especially with regard to the capacitive decoupling at the gate and drain terminations. The layout was completed in a matter of minutes, using the “snap together” function available in AWR, leaving only the surrounding metal and drill holes to be placed. The layout is shown in Figure 3.

**Fabrication**

The amplifier was designed from Rogers 4003 PCB material. This material was chosen for its good RF characteristics and ease of manufacture. The PCB was milled out in the electronics workshop at the university and loaded by hand.

CAD software was used to design a small aluminum heat sink. This was manufactured by the mechanical workshop. As well as providing some heat sinking for the transistor, it was used to ground the source of the HEMT and provide a solid mounting for the transistor. It was also used at the input and output to hold the SMA connectors.

**Measurements**

After taking a few manual measurements and seeing the difference that a few tenths of a dB in calibration accuracy had on the efficiency, it was decided to use VB.NET and program an automated test setup that included calibration for all the instruments.

A soft instrument was created to measure the PAE. This program allows the frequency, input power, drain voltage, and bias level to be swept. Using a power meter, values are obtained to correct differences between requested/
measured power and actual power. These are entered into the graphical user interface (GUI) and are used in the PAE calculation.

A screen-shot of the GUI is shown in Figure 4. Communication with the instruments is handled using the GPIB. This software allows the amplifier to be characterized easily. The bias point, input power level, and frequency of highest efficiency are also able to be determined.

Simulated versus Measured Results
With the measurements done, simulated versus measured results could now be analyzed (see Figure 5). The efficiency and output power levels were extremely close to specification, especially across the frequency desired for this design. A slight error in the calibration shows the measured PAE to be slightly higher than that measured at the competition.

The simulated output current and voltage waves are shown in Figure 6. It appears, due to the voltage peaking, that this amplifier is operating in a quasi-F⁻¹ mode. It is likely that there is a portion of Class E operation as well due to the output capacitance within the device and the capacitance added by the packaging. As Steve Cripps mentions in the introduction to his latest book [5], it is difficult to determine the class unless the output current and voltage waves can be directly measured. To compound this, these simulation results are not the intrinsic transistor current and voltage waveforms since they are measured outside the package.

Conclusion
The competition was a great experience. Designing and building an amplifier is a great way to learn (Figure 7). It is also a refreshing change from integrated circuit design as the amplifier can be tweaked, transmission lines can be modified if needed, and it can be held firmly in two hands!

The measurement problems encountered on the competition day indicate how important it is to verify the measurement setup through a known standard or some other method; it also demonstrates that taking an accurate PAE measurement is quite difficult—a few tenths of dB error in the output signal equates to a lot of percentage points!

I would encourage other students to enter this competition as it is a rewarding experience and gives you the opportunity to design and build a real amplifier.

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