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High-frequency TSV Failure Analysis and Detection Method with Z-parameter

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Abstract

This paper introduces a novel TSV failure analysis and detection method with high-frequency measurement of $Z$ parameter. To improve fabrication yield of a 3D IC, this paper proposes a novel electrical test method how three types of TSV failures such as connection failure, insulator failure and conductor failure can be detected and differentiated by using high frequency modeling, analysis and measurement of $Z_{11}$ magnitude. Based on the failure modeling and analysis, the failure masks which can differentiate failure types are also proposed. The sensitivity of the proposed failure masks are conducted by considering fabrication process variations.

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1. Introduction

As the through-silicon via (TSV) enables wide input/output (I/O) application for the higher system bandwidth and 3-dimensional integration of multiple chips, TSV-based 3D IC system becomes a promising solution to high-end multi-chip systems. Especially, many of mobile and graphic application systems require higher system bandwidth as well as lower power consumption. Therefore, high-speed signaling, low-power consumption, wide I/O availability of a TSV serve as key drivers for adoption of a 3D IC and TSV interconnect solution in the market [1-2]. In order to maximize system performance with TSVs, many researches have been done such as modeling and characterization of a TSV [3-5] or design of guidelines for low power consumption, low noise and low insertion loss of a TSV-based I/O channel [6-8]. Based on the previous researches, we can conclude that TSV is a very good and highly performing interconnect which not only provides vertical link but also guarantees high-speed signaling due to the short interconnection lengths and small TSV diameter under 10 µm.

![Fig.1 3-dimensional integrated circuit (3D IC) system with homogeneous and heterogeneous dies which has several µm order TSV diameter and hundreds of µm thickness of the stacked chips.](image)

However, the critical bottleneck of a TSV-based 3D IC is the final 3D IC yield which restrains the growth of the 3D IC market. To integrate ICs vertically, many of fabrication processes are needed: TSV fabrication, wafer/die thinning, wafer/die alignment, and wafer/die stacking. The yield loss from each fabrication process during 3D IC manufacturing directly affects to the overall system reliability. Three types of failures are currently investigated as critical defects to be solved: connection failure between stacked chips (open/short defect), TSV oxide failure (impurity inside the insulation layer or breakdown of the oxide liner), and TSV void or die misalignment failure (resistive defect). Due to these failures, a 3D IC can be functionally failed and the signal integrity cannot be guaranteed. In addition, since TSV count is required to be increased up to several hundred for higher system bandwidth, the 3D IC yield problem becomes more serious. As shown in Fig. 2, the final 3D IC yield is severely decreasing as the number of TSVs per a chip increases. Especially, chip yield starts to decrease sharply with more than 1k ea TSVs. In order to improve the reliability of 3-dimensionally integrated system, a novel non-destructive testing method is strongly needed which can figure out what kind
In this paper, a novel non-destructive failure detection method using $Z$ parameter is proposed in order to differentiate failure types and also to localize the failure in TSV-based 3D ICs. In order to electrically detect failures, it is necessary to study and analyze electrical characteristics of failures in advance. Thus, modeling and analysis of TSV failures are conducted with $Z$ parameter. The failure models of a defected TSV are proposed with lumped RLGC components. On the basis of the proposed equivalent circuit model, $Z_{11}$ magnitude of a TSV with failures is analytically derived. Based on the frequency-domain analysis of TSV failures, a novel failure detection method is proposed by comparing $Z_{11}$ magnitudes from the defected TSV and the normal TSV. In order to experimentally verify the proposed method, test samples which have intentional defects along the TSV channel are fabricated and measured using Vector Network Analyzer (VNA). In addition, sensitivity of the proposed detection method is analyzed by considering the fabrication process variation, especially physical dimension variation. Based on the sensitivity analysis of the proposed test method, the applicability and the limitation of the proposed test method are also discussed.

2. Principle of the Proposed Novel High-Frequency TSV Failure Detection Method

In order to detect TSV failures electrically, the proper electrical parameter has to be determined which is able to characterize the electrical feature of the failure. In addition, it is preferred to differentiate the failure type among various types of failures with the same electrical parameter for the simplicity of the test. Thus, a novel non-destructive TSV failure detection method is proposed which requires only one port RF measurement of $Z_{11}$ magnitude for not only the failure detection but also the failure-type differentiation. As for the failure detection criterion, the reference $Z_{11}$ magnitude is needed which is the
Z_{11} magnitude from the defect-less TSV or TSV channel. Based on the comparison between the reference $Z_{11}$ magnitude and the measured $Z_{11}$ magnitude of the test sample, we can test whether the sample is failed or not. The comparison of the $Z_{11}$ magnitudes can be done by subtracting the measured one from the reference in dB scale. Then, we can get $\Delta Z_{11}$ magnitude as for the failure detection criterion. To simply detect failures and differentiate failure types, the failure masks are designed and proposed in this paper. Each failure mask is designed based on the feature of the $\Delta Z_{11}$ magnitude for each failure type. Therefore, after comparing the $\Delta Z_{11}$ magnitude to the failure masks, we can test TSV or TSV channel whether the defect exists or not and also which type of the defect exists. Three types of failures are considered in this paper; connection failure (open/short defect), insulator failure (leakage), and void or die misalignment failure (resistive defect).

![Figure 3 Concept of the proposed TSV failure detection method using $Z_{11}$ magnitude difference between the reference and the defected one based on one port RF measurement using VNA.](image)

Figure 3 shows the test environment of the proposed test method. The proposed test method requires one port contact probing on the 3D chip or wafer using Vector Network Analyzer (VNA). As shown in Fig. 3, it does not require any additional active test scheme for the test. Furthermore, since it requires only one port measurement, this test method is applicable at every process step before back-grinding, after back-grinding and also after stacking only if probe can be directly contacted where to be tested.

3. TSV Failure Modeling and Analysis using Z parameter

In order to electrically detect and differentiate TSV failures along the TSV-based channel in a stacked-chip, electrical characteristics of TSV failures have to be analyzed in advance. On the basis of the electrical model and analysis of a normally fabricated TSV and a TSV with failures, key electrical characteristics for the failure detection are extracted from the Z-parameter analysis and measurement. Z parameter has been selected as the failure-detecting parameter, because it provides the information of the capacitive and the inductive characteristic more intuitively than S parameter.

3-1. High-frequency Modeling and Analysis of a defect-less TSV

Since TSV is a capacitive dominant channel due to the SiO2 insulation layer of a TSV, overall characteristic of a TSV up to 20 GHz shows capacitive-dominant behavior. Figure 4 describes $Z_{11}$ magnitude behavior as frequency increases up to 20 GHz. Depending on
the frequency regions, the dominant electrical RLGC component of a TSV is characterized. Since oxide capacitance of a TSV, \( C_{ox} \), is the most dominant parasitic capacitance, \( C_{ox} \) dominantly determines the \( Z_{11} \) magnitude in low frequencies, region A. As frequency increases, frequency-independently flat region of the \( Z_{11} \) magnitude in region B is determined by loss term, conductance of the silicon substrate, \( G_{Si} \). Over 10 GHz in region C, the relatively smaller capacitances such as \( C_{Si}, C_{IMD}, C_{bump} \) determine the electrical behavior of \( Z_{11} \) magnitude of a TSV. For the equivalent impedance, the analytic equation with lumped RLGC components for the equivalent impedance of a TSV, \( Z_{eq,TSV}(\omega) \), is presented in equation (1). With \( Z_{eq,TSV}(\omega) \), \( Z_{11}(\omega) \) in dB can be calculated as shown in equation (2).

\[
Z_{eq,TSV}(\omega) = R_{eq}(\omega) + \omega \cdot L_{eq} + \frac{\sigma_{Si}}{\varepsilon_{Si}} \left( C_{ox} C_{Si} + 2C_{Si}C_{IMD,bump} \right) + \omega \left( C_{ox} \left( C_{Si} + C_{IMD,bump} \right) + 2C_{Si}C_{IMD,bump} \right)
\]

(1)

\[
Z_{11}(\omega) \text{ [dB]} = 20 \log_{10} \left( Z_{eq,TSV}(\omega) \right)
\]

(2)

Based on the analysis of the TSV with or without defect, we can compare and detect different electrical behaviors of the failed cases from electrical modeling and analysis. By the reference measurement and analysis, we can characterize the different electrical behavior of TSV failures compared to the reference. Based on the equivalent circuit modeling with lumped elements, the electrical characterization of the TSV failures is conducted. In this section, high-frequency modeling and analysis of three types of failures are conducted by simulations with 3D field solver, Ansoft HFSS. Depending on the failures, the impacts on the \( Z_{11} \) magnitude with each defect are characterized. Three types of failures will also be electrically modeled and analyzed discussed in this paper; connection failure (open/short defects), insulator failure (leakage), and void or die misalignment failure (resistive defect).
3-2. High-frequency Modeling and Analysis of Connection Failure (Open)

In case of connection failure, there are two types which are open and short defects. Open defect at the connection between the stacked dies can be occurred when the top or bottom side of the TSV, solder bump or bumping pad is oxidized during the fabrication processes. As a result, the physical and electrical connection is not well done due to the oxidized layer between the connecting parts.

For a full disconnection failure where there are open defects between the stacked dies, the disconnected part is modeled as a series capacitance along the TSV channel as shown in Fig. 5(a). In Fig. 5(a), $Z_{eq,TSV}(\omega)$ represents the equivalent impedance of a TSV which is dependent on frequencies. Due to the series capacitance, $Z_{11}$ magnitude of the failed case has higher values than that of the normal case. The $\Delta Z_{11}$ magnitude is extracted by subtraction of the $Z_{11}$ magnitude of the defected TSV channel from that of the normal one. As a result, the values of the extracted $\Delta Z_{11}$ magnitudes are all positive in all frequencies up to 20 GHz as shown in Fig. 5(b). In addition, $\Delta Z_{11}$ magnitudes of the defected channel become smaller as frequency increases, because the impedance of the series capacitance due to the disconnection gets smaller as the frequency increases. As a result, $\Delta Z_{11}$ magnitude in region C closes to zero which means that $Z_{11}$ magnitude of the defected case closes to that of the normal case.

If we analytically model the equivalent impedance in case of disconnected TSV channel, $Z_{eq,disconnect}$, the $Z_{eq,disconnect}$ with the lumped RLGC components in the equivalent circuit model is proposed in equation (3). As shown in (3), $Z_{eq,disconnect}$ is always larger than $Z_{eq,TSV}$ in region A. In addition, since $Z_{eq,disconnect}$ is still proportional to $\omega^{-1}$, the slope of the $Z_{11}$ magnitude of the disconnected TSV channel in region A is -20 dB/decade.

$$Z_{eq,disconnect}(\omega) = \frac{2 + \omega \cdot C_{disconnect}}{\omega \cdot C_{ox}} > Z_{eq,TSV}(\omega) \text{ in region A} \quad (3)$$

![Fig. 5 (a) Equivalent circuit model of a two stacked TSVs with connection failure as an open defect and (b) the resulting Z11 magnitudes as the amount of the disconnection varies which is represented as series capacitance, C_disconnect.](image)
3-3. High-frequency Modeling and Analysis of Connection Failure (Short)

As the system requires higher bandwidth, pitch between I/Os becomes shorter in order to maximize I/O count with the limited die area which results in fine-pitch integration of high number of I/Os. In addition, fine-pitch micro-bumps are necessary to connect the stacked dies. The short defect in a TSV channel can be occurred when the fine-pitch bumps are shorted due to the miss control the amount of the solder compound or the stacking. With the shorted case, shorted part can be modeled as a conductance between the signal and ground node. Thus, the equivalent circuit model is proposed as shown in Fig. 6(a). The resulting $Z_{11}$ magnitude with short defect is shown in Fig. 6(b). Since short defect which is modeled as shunt resistance, $R_{\text{short}}$, provides low impedance path to the ground, $Z_{11}$ magnitude is always lower than the reference. And if $R_{\text{short}}(\omega)$ is much smaller than $Z_{\text{eq,TSV}}(\omega)$, the equivalent impedance of a TSV with short defect is simplified as $R_{\text{short}}(\omega)$ as shown in equation (4).

$$Z_{\text{eq,short}}(\omega) = Z_{\text{eq,TSV}}(\omega) || R_{\text{short}}(\omega) \approx R_{\text{short}}(\omega) \quad (4)$$

(4) is satisfied when $R_{\text{short}}(\omega)$ is much smaller than $Z_{\text{eq,TSV}}(\omega)$.

3-4. High-frequency Modeling and Analysis of Insulator Failure

Insulator failure is a defect inside the insulation layer surrounding via of a TSV. With an insulator failure, the equivalent circuit model is proposed as shown in Fig. 7(a). If there are impurities or cracks inside the insulation layer or break downs occur, conductance, $G_{\text{ox,defect}}$, has to be added in parallel to the oxide capacitance, $C_{\text{ox}}$, to the equivalent circuit model. The values of $G_{\text{ox,defect}}$ change depending on the properties of the defect. In Fig. 7(b), $\Delta Z_{11}$ magnitudes are plotted as $G_{\text{ox,defect}}$ varies. Since the capacitance from the insulation layer is the most dominant one among the parasitic
capacitances of a TSV, it dominantly determines the electrical behavior of the $Z_{11}$ magnitude in low frequencies, in region A, as shown in Fig. 4. $C_{\text{ox}}$ is about hundreds of fF order and other parasitic capacitances such as $C_{\text{Si}}, C_{\text{IMD}},$ and $C_{\text{Bump}}$ are several to tens of fF order. Thus, the $Z_{11}$ magnitude of a TSV with an insulator failure differs from the reference only in region A. As a result, $\Delta Z_{11}$ magnitudes are only shown in region A. However, $Z_{11}$ magnitude with an insulator defect is smaller than that of the normal one due to the leakage through the $G_{\text{ox,defect}}$. As a result, $\Delta Z_{11}$ magnitudes are all negative in region A when there is an insulator failure. Based on the analytical modeling of the equivalent impedance of a TSV with insulator defect, $Z_{\text{eq,defect}}$, at low frequencies, we can confirm that $Z_{\text{eq,defect}}$ is always smaller than $Z_{\text{eq,TSV}}$ as shown in equation (5). In addition, $Z_{\text{eq,defect}}$ does not have $-20$ dB/decade capacitance slope, because $Z_{\text{eq,defect}}$ is not directly proportional to $\omega^{-1}$.

\[
Z_{\text{eq,defect}}(\omega) \approx \frac{2}{\omega \cdot C_{\text{ox}} \left(1 + \frac{\sigma_{\text{ox,defect}}}{\omega \cdot C_{\text{ox,defect}}}\right)} < \frac{2}{\omega \cdot C_{\text{ox}}} \approx Z_{\text{eq,TSV}}(\omega) \text{ in region A} \quad (5)
\]

where, $G_{\text{ox,defect}} = C_{\text{ox}} \cdot \frac{\sigma_{\text{ox,defect}}}{\varepsilon_{\text{ox,defect}}} \quad \text{and} \quad C_{\text{ox}} \gg C_{\text{Si}}, C_{\text{IMD/BS}}$

### 3-5. High-frequency Modeling and Analysis of Void or Alignment Failure

In case of a partial connection due to the misalignment between the stacked dies or voids inside TSVs or bumps, the equivalent impedance of a TSV-based channel increases since the resistance of the partially connected part is added to that of the normal one. As a result, $R_{\text{void}}$ is added for the equivalent circuit modeling of the TSV channel with voids or die misalignment failure as shown in Fig. 8(a). The resulting $Z_{11}$ magnitude of the defected case has higher values than the normal one due to the increased series resistance. Consequently, $\Delta Z_{11}$ magnitudes are all positive in all frequencies up to 20 GHz as shown in Fig. 8(b). The equivalent impedance is presented with $R_{\text{void}}$ in equation (6).
4. Proposed TSV Failure Masks for the Failure Type Differentiation

4-1. Proposal of TSV Failure Masks

To detect TSV failures on the basis of the frequency-domain measurement results, the failure detection criteria must be clearly defined. From the analysis results of TSV channels with or without defects, it can be noticed that the electrical characteristics of TSV failures appear differently depending on the failure types and frequency regions. Thus, they can be differentiated with $\Delta Z_{11}$ magnitude variation as frequency varies. The $\Delta Z_{11}$ magnitude is calculated by subtracting the $Z_{11}$ magnitude of the normal channel from that of the DUT to be tested. With the $Z_{11}$ magnitude differences, failure masks for the failure type are designed. Since $\Delta Z_{11}$ magnitude is used as a test signal, we will call it as $Z_{11,\text{test}}(\omega)$ which varies as frequency varies. And $Z_{11,\text{test}}(\omega)$ is defined in equation (7).

$$Z_{eq,\text{void}}(\omega) = Z_{eq,TSV}(\omega) + R_{\text{void}}(\omega) \quad (6)$$

4-2. Proposed Failure Mask for Connection Failure (Open)

Since $Z_{11}$ magnitude of the disconnected case is always larger than that of the defectless TSV channel, $Z_{11,\text{test}}$ have positive values in all frequencies as shown in Fig. 9. However, since the impedance of the series capacitance from the disconnected part decreases as the frequency increases, $Z_{11,\text{test}}$ becomes smaller as frequency increases. Thus, the failure mask for the disconnection failure is designed as constant and positive $Z_{11,\text{test}}$ in region A but decreasing $Z_{11,\text{test}}$ in region B and C. Thus, $Z_{11,\text{test}}$ at low frequency
is always bigger than the $Z_{11,\text{test}}$ at high frequency. Since the equivalent impedance of the disconnected TSV channel is still proportional to $\omega^{-1}$, the slopes of the $Z_{11}$ magnitudes of the disconnected TSV channel and the normal channel are the same which is -20 dB/decade. As a result, $Z_{11,\text{test}}$ in region A is flat as frequency varies in region A.

4-3. Proposed Failure Mask for Connection Failure (Short)

In case of the connection failure with short defect between signal and ground, the $Z_{11}$ magnitude is lower than that of the normal TSV channel only in all frequencies up to 20 GHz. Thus, the failure mask for the short defect is designed as an increasing negative $Z_{11,\text{test}}$ as frequency increases up to 20 GHz as shown in Fig. 10.
4-4. Proposed Failure Mask for Insulator Failure

In case of the insulator failure, the $Z_{11}$ magnitude is lower than the reference only in region A. Thus, the failure mask for the insulator failure is designed as increasing negative $Z_{11,\text{test}}$ only in region A as shown in Fig. 11. Thus, it has a triangular shape as for the criterion to differentiate the insulator failure.

![Fig. 11 The proposed failure mask in case of the insulator failure which is only negative at low frequencies in region A and becomes zero in region B and C.](image)

4-5. Proposed Failure Mask for Conductor Failure (Void or Misalignment)

In case of the void or die misalignment failure, the $Z_{11}$ magnitude is always larger than the reference. Thus, the failure mask for the conductor failure such as void or partial connection is designed as increasing positive $Z_{11,\text{test}}$ as frequency increases up to 20 GHz. However, the conductor failure is the hardest one to detect electrically among various types of TSV failures since it does not bring the considerable impact on the electrical behavior of a TSV.

![Fig. 12 The proposed failure mask in case of the conductor failure such as void or partial connection which is all positive and increases as frequency increases.](image)
5. Sensitivity Analysis of the Proposed Method

The capacitance of an oxide liner surrounding TSV is the most dominant capacitance of a TSV. Thus, the physical parameters which determine the oxide capacitance, $C_{ox}$, which are TSV diameter ($d_{TSV}$), TSV height ($h_{TSV}$) and oxide thickness ($t_{ox}$) are considered in the sensitivity analysis. Compared to other physical parameters, the variation of these three parameters affects more to the $Z_{11}$ magnitude variation of a TSV. The plotted $\Delta Z_{11}$ magnitudes are extracted by comparing $Z_{11}$ magnitudes with process variations to that of a well-fabricated TSV which has originally intended dimensions.

Due to unstable via etching processes, fabricated $d_{TSV}$ may differ from the original design value. $\Delta d_{TSV}$ of 1 $\mu$m corresponds to the TSV diameter variation range with maximum 10 % error when $d_{TSV}$ is originally designed as 10 $\mu$m. With $\Delta d_{TSV}$ of 1 $\mu$m, $Z_{11}$ magnitude varies by at most 0.4 dB as shown in Fig. 13.

\[ Z_{11} \text{ magnitude variation depending on TSV diameter variations from 9 to 11 } \mu m \text{ and (b) the resulting } \Delta Z_{11} \text{ magnitudes which are the differences from the reference } Z_{11} \text{ magnitude with } d_{TSV} \text{ of 10 } \mu m. \]

\[ Z_{11} \text{ magnitude variation depending on TSV oxide thickness variations from 0.3 to 0.5 } \mu m \text{ and (b) the resulting } \Delta Z_{11} \text{ magnitudes which are the differences from the reference } Z_{11} \text{ magnitude with } t_{ox} \text{ of 0.5 } \mu m. \]
Due to the unstable insulation layer deposition processes, $t_{ox}$ can be different from the originally designed value as shown in Fig. 14. $\Delta t_{ox}$ of 0.1 μm corresponds to the maximum 20% error when $t_{ox}$ is assumed as 0.5 μm. With $\Delta t_{ox}$ of 0.1 μm, $Z_{11}$ magnitude differs by 1 dB. In addition, $h_{TSV}$ may differ from the originally designed value because the unstable wafer thinning process results in the non-uniform substrate thickness across a wafer. Consequently, the thickness at the center of the wafer and the edge of the wafer may be different. $\Delta h_{TSV}$ of 5 μm is the height variation range with the maximum 10% error when $h_{TSV}$ is assumed as 50 μm. As shown in Fig. 15, with $\Delta h_{TSV}$ of 5 μm, $Z_{11}$ magnitude differs by 0.7 dB as maximum under 1 GHz and 1 dB at high frequencies.

**Fig. 15** (a) $Z_{11}$ magnitude variation depending on TSV height variations from 45 to 55 μm and (b) the resulting $\Delta Z_{11}$ magnitudes which are the differences from the reference $Z_{11}$ magnitude with $h_{TSV}$ of 50 μm.

**Fig. 16** The sensitivity mask, $Z_{11,\text{sen}}$, is designed as ±1 dB in all frequencies when assuming that the physical dimensions may change with the error of maximum 10% with $d_{TSV}$ of 10 μm, $h_{TSV}$ of 50 μm and $t_{ox}$ of 0.5 μm.

Even though there are $Z_{11}$ magnitude variations depending on process variations, the proposed failure masks are still valid since those process variations bring parallel level
shift of $Z_{11}$ magnitudes due to the capacitance difference depending on process variations. As a result, those process variation effects do not require redesign of the proposed failure masks, however, the valid failure detecting range may be reduced. Therefore, the failure mask requires maximum $\pm 1$ dB margin when considering maximum 10% variation of TSV design parameters as shown in Fig. 16. If the process becomes more stable and the maximum error rate is lowered, the sensitivity mask can be shrink more which results in the reduced margin for the sensitivity consideration represented as $|Z_{11,\text{sen}}[\text{dB}]|$. Then the possible failure detecting range may be enlarged as $|Z_{11,\text{sen}}[\text{dB}]|$ decreases. As $|Z_{11,\text{sen}}[\text{dB}]|$ decreases more, the smaller defects can be detected. When detecting failures with $Z_{11,\text{test}}$, $Z_{11,\text{sen}}$ has to be considered together for the higher accuracy.

6. Test Flow of the Proposed Failure Detection Method

Based on the modeling and analysis of the electrical characteristic of $Z_{11}$ magnitude, the novel TSV failure test method is proposed. As shown in Fig. 17, the test flow is summarized as a chart. The test signal, $Z_{11,\text{test}}(\omega)$, is firstly extracted by the subtracting $Z_{11,\text{ref}}(\omega)$ which is the reference $Z_{11}$ magnitude of the defect-less one from the $Z_{11}$ magnitude of the sample to be tested, $Z_{11,\text{ref}}(\omega)$.

The next step is to check $Z_{11,\text{test}}(\omega)$ with the sensitivity mask, $Z_{11,\text{sen}}(\omega)$, which is designed with the maximum error rate of the physical dimension and the default parameter dimensions. If the $Z_{11,\text{test}}(\omega)$ is included in the range of $Z_{11,\text{sen}}(\omega)$, the test is

![Test flow of the proposed TSV failure test method](image-url)
over at this step since it is confirmed as a defect-less one. If \( Z_{11,\text{test}}(\omega) \) is not included in the range of \( Z_{11,\text{sen}}(\omega) \), we can be noticed that the sample is a failed one.

Next following steps are to detect what kind of failure exists in the sample. First step for the failure differentiation is to check \( Z_{11,\text{test}}(\omega) \) in all frequencies up to 20 GHz is positive or not. If positive, there are two possibilities; open defect and conductor defect such as void or partial connection due to the die misalignment. If the value subtracting \( Z_{11,\text{test}} \) (high frequency over 15 GHz) from \( Z_{11,\text{test}} \) (low frequency under 0.01 GHz) is positive, then the failure type is the open defect. Because it means that \( Z_{11,\text{test}} \) decreases as frequency increases. But if this value is negative, it means that \( Z_{11,\text{test}} \) increases as frequency increases. Thus, it is the conductor defect.

If \( Z_{11,\text{test}} \) is not all positive up to 20 GHz, it can be negative. In this case, there are two possible failure types; short defect and insulator defect. These two types of failures can be differentiated by using the feature of the insulator failure. In case of insulator failure, \( Z_{11,\text{test}} \) over 1 GHz is almost zero. Therefore, we can differentiate them by checking whether \( Z_{11,\text{test}} \) over 1 GHz has more negative values than \( Z_{11,\text{sen}} \) over 1 GHz or not.

As a result, electrical modeling and analysis of TSV failures with \( Z_{11} \) magnitude, we can not only detect failures but also differentiate the failure type.

7. Fault Localization using the Proposed Method

If we assume that the same amount of the specific failure is generated at any location, we can apply this proposed method for the fault localization. Depending on the failure location, equivalent impedances seen at the probing port appear different. Thus, \( Z_{11} \) magnitudes depending on the fault locations are differently shown. The base-line structure for the analysis is GSG-type single-ended TSVs with TSV diameter of 10 µm, TSV height of 50 µm, TSV oxide thickness of 0.5 µm and TSV pitch of 40 µm.

![Fig. 18 Z₁₁ magnitudes depending on disconnection location along the four-stacked TSVs. As the distance between the probing point and the disconnected point gets shorter, the level of Z₁₁ magnitude gets higher due to the high impedance of the series disconnection capacitance at the disconnection point.](image)
Figure 18 shows the $Z_{11}$ magnitudes depending on disconnection location along the four-stacked TSVs. Disconnection is intentionally made with the thin oxide layer at the bottom side of the signal bump. Thickness of the oxide layer for the disconnection is 0.5 µm. Since the disconnection is electrically modeled as a series capacitance between the stacked TSVs, the impedance with open defect is higher than the reference. Thus, as the disconnection location becomes closer from the probing point, the impedance seen from the probing point increases. As a result, if we assume that the amount of the open failure

![Figure 19](image_url)  
**Fig. 19** $Z_{11 \text{,ref}}$ depending on disconnection location along the four-stacked TSVs. As the distance between the probing point and the disconnected point gets shorter, the level of $Z_{11 \text{,ref}}$ gets higher.

![Figure 20](image_url)  
**Fig. 20** $Z_{11}$ magnitudes depending on short defect location along the four-stacked TSVs. As the distance between the probing point and the disconnected point gets shorter, the level of $Z_{11}$ magnitude gets lower due to the low impedance of the shunt short conductance at the shorted point.

Figure 18 shows the $Z_{11}$ magnitudes depending on disconnection location along the four-stacked TSVs. Disconnection is intentionally made with the thin oxide layer at the bottom side of the signal bump. Thickness of the oxide layer for the disconnection is 0.5 µm. Since the disconnection is electrically modeled as a series capacitance between the stacked TSVs, the impedance with open defect is higher than the reference. Thus, as the disconnection location becomes closer from the probing point, the impedance seen from the probing point increases. As a result, if we assume that the amount of the open failure
is the same due to the same fabrication environment, we can localize disconnection location by using the failure masks from $Z_{11,\text{test}}$ as shown in Fig. 19.

Figure 20 shows the $Z_{11}$ magnitudes depending on short-defect location along the four-stacked TSVs. Short defect is intentionally made by shorting signal and ground bumps. Depending on short location, $Z_{11}$ magnitudes are differentiated due to the different equivalent impedances for each case. As the location of the short becomes closer from the probing point, $Z_{11}$ magnitude lowers. $Z_{11,\text{test}}$ are plotted depending on short location along the stacked TSVs in Fig. 21. Depending on the short defect location, $Z_{11,\text{test}}$ is different.

As a result, fault localization is possible with the proposed test method. However, if the amount of the defect is not the same, it becomes hard to differentiate failure location.

**Experimental Verification of the Fault Localization using the Proposed Method**

For the experimental verification, we fabricated the GSG-type single-ended TSV daisy chains with open defects by intentionally designing disconnection. Figure 22 shows the fabricated defected TSV daisy chain by missing metal via between TSV and metal line. For the analysis the effect of the failure location variation, the samples are fabricated with two cases (Case 1, 2). Case 1 has missed the closest metal via from the probing point. Case 2 has missed the secondly closest metal via from the probing point. In addition, only the metal via along the signal line is missed at each case. Thus, two ground lines nearby a signal line are all normally connected without any defect. For the fabricated TSV structure, $d_{\text{TSV}}$ is 40 $\mu$m, $h_{\text{TSV}}$ is 64 $\mu$m, $t_{\text{ox}}$ is 0.3 $\mu$m and TSV pitch ($p_{\text{TSV}}$) is 250 $\mu$m. The fabricated bump has a height of 22 $\mu$m and a diameter of 150 $\mu$m. High-frequency
measurements are conducted using Vector Network Analyzer (VNA) and microprobes. $Z_{11}$ magnitudes are measured up to 20 GHz.

Fig. 22 The cross-sectional view and the SEM pictures of the fabricated TSV daisy chain with an open defect by missing a metal via between the metal line and the TSV.

Fig. 23 Measured $Z_{11}$ magnitudes of the normal and the defected TSV daisy chains (Case 1 and 2) and the equivalent circuit expressions depending on the cases with $Z_{eq,TSV}$ and $C_{disconnect}$.

Figure 23 shows the measured $Z_{11}$ magnitudes with the fabricated defected TSV daisy chains (Case 1, 2) with an open defect by omitting a metal via. Solid line shows measured $Z_{11}$ magnitude of the normal one. Dotted line and dashed line shows $Z_{11}$ magnitudes of the defected cases. For the Case 1, the closest metal via from the probing point is missed. As shown in dotted line in Fig. 23, series capacitance effect due to the disconnection in Case 1 is appeared dominantly in all frequency ranges. In Case 1, if the disconnection
capacitance, $C_{\text{disconnect}}$, increases, for example if disconnection gap gets smaller, $Z_{11}$ magnitude level decreases. In the Case 1, the value of series capacitance is small which is about tens of fF so that it affects $Z_{11}$ magnitude up to 20 GHz. In Case 2, second metal via from the probing point is missed. Since the series capacitance due to the disconnection of the second metal via is located further from the probing point, $Z_{11}$ magnitude is lower than that from Case 1. In addition, the impedance of the series capacitance gets lower as frequency increases. Thus, $Z_{11}$ magnitude difference between disconnected cases (Case 1, Case 2) and normal case gets smaller as frequency increases. From the measurement results, we verified that as the disconnection which is electrically open at DC locates closer from the probing point, $Z_{11}$ level gets higher. Thus, Case 3 has the lowest $Z_{11}$ magnitude level among the three cases and Case 2 and 1 has the higher level of $Z_{11}$ magnitude.

8. Multiple-Failure Detection using the Proposed Method

Due to the various unstable fabrication processes, more than two types of failures can be occurred in one TSV-based channel. Thus, the applicability of the proposed test method is analyzed for the multiple-failure detection. Four-stacked TSV with open and insulator defects is considered as the base-line structure which is the same in previous analyses. $Z_{11}$ magnitudes depending on the disconnection locations with the same insulator defect in a TSV on 1st tier are shown in Fig. 24. Since the amount of the insulator failure is applied as the same for each case, the DC losses due to the insulator defect are the same for all the cases. Thus, $Z_{11}$ magnitudes of all cases at 0.01 GHz converge to the same value about 84 dB. However, over 1 GHz, $Z_{11}$ magnitudes follow different $Z_{11}$ magnitudes depending on disconnection locations.

![Fig. 24 $Z_{11}$ magnitudes depending on disconnection location variation along the four-stacked TSVs when insulator defect is applied as the same on 1st tier for each case.](image)

*Default defect: Insulator defect in a TSV on 1st tier*
Figure 25 shows $Z_{11, \text{test}}$ depending on disconnection location variation along the four-stacked TSVs when insulator defect is applied to all cases as the same amount on 1st tier. At low frequencies under 1GHz, the failure mask of the insulator failure is applicable. Over 1 GHz, the failure mask of the disconnection failure is applicable. As a result, even though multiple failures are mixed in one channel, the electrical features of each failure type are clearly appeared in the $Z_{11}$ magnitude. Therefore, depending on frequency ranges, the multiple failure masks can be applicable to $Z_{11, \text{test}}$ for the detection of the specific type of the failure among multiple failures.

9. Limitations of the Proposed Failure Detection Method

The proposed failure analysis and detection method only requires one-port RF measurement, thus, it is very simple and also applicable, at every process step regardless of TSV process types. However, it requires direct probing; thus, it is needed to design probing pad for the test, or, we have to directly contact TSVs or bumps for the test. But, it can harm the surface of a TSV or a bump due to the contacted marks from the probing.

In addition, if we are to test a TSV or a TSV channel, GS or GSG-type probe is used to test. However, one contact probing provides a $Z$ parameter of one channel. Therefore, it requires fast probing at best all in parallel in order to test high number of TSVs in a chip or a wafer. Since, TSV-based 3D IC is designed with high number of I/Os for the higher system bandwidth, testing time becomes an important factor which has to be considered.

In order to reduce the parallel probing time when using the proposed test method, we can use wide I/O probe cards which provide proper electrical probe contact at fine-pitch micro-bumps with new metallurgies for realistic array sizes and with limited probe damage so as not to impair downstream bonding [10].
10. Conclusions

In this paper, the novel high-frequency failure analysis and detection method using $Z$ parameter is proposed. As for the failure detection and differentiation criteria, failure masks are designed and proposed depending on failure types and locations. Based on the sensitivity analysis with the fabrication process variation resulting in the physical dimension variation, test flow chart is summarized how to detect TSV failures and differentiate failure types using the proposed method. With the proposed method, fault localization is conducted and verified by high-frequency measurements with the fabricated test samples. In addition, the applicability of the multiple failure detection and the practical limitation of the proposed method are analyzed and discussed.

References