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Methods for Discovering and Mitigating Switching Regulator Noise Coupling for Complex PCB System

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Abstract
Server boards and other complex PCB systems are experiencing more densely routed IOs and have an increasing number of power rails that make it challenging to control switching voltage regulator (VR) noise. Our server board design flow has been required to address increasing occurrences of reduced signal margin, memory failures, unreliable booting and system hangs. In this paper we describe multiple VR noise coupling mechanisms we have observed in our server board designs and our application of various analysis methods to discover the root cause and mitigate VR noise coupling issues. We share our comparisons for multiple designs of analysis versus lab measurements and also discuss near field scanning measurements, which have discovered further potential coupling mechanisms.

Author(s) Biography
Amy Luoh received the B.S. and M.S. degree in electrical and computer engineering from Oregon State University. She has been working as a signal integrity engineer in server board design group at Intel since 2005. She performs routing reviews, signal integrity related simulations and measurements for the server board designs. She has been especially involved in the study of power noise coupling analysis into signals.

Xiaoning Ye is currently a senior analog engineer with Intel Corporation, where he is a technical lead working on signal integrity of high speed differential interconnect in Intel Server systems. Xiaoning Ye received his Bachelor and Master Degrees in electronics engineering from Tsinghua University, Beijing, China, in 1995 and 1997 respectively, and Ph.D degree in electrical engineering from University of Missouri – Rolla (currently Missouri University of Science and Technology) in 2000. He has published over 30 IEEE papers, and holds 4 patents and 2 patent applications.

Jiangqi He received his B.S. in Physics from Xiamen University 1992 and Ph.D. from Duke University 2000 in the field of computational electromagnetic, respectively. He joined electrical core competency team at Intel since then. He has been worked on power integrity, high speed signaling and EMI for computer system by focusing on silicon, package, socket and platform level interconnect technologies. He is now interested in advance technologies for system level power delivery and power integrity and their relations with high speed signaling. He holds more than 20 US patents and has published more than 30 technical papers.

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Muhammed Elgousi is currently employed by Intel Corporation as an Analog Engineer, working in the Atom and SOC design group. His primary focus is on low power analog circuit design on the newest Intel Atom processor. Muhammed joined Intel in 2006 and worked on Intel Servers CPU Power delivery and embedded voltage regulators. He received a B.S. degree in Electrical Engineering from Arizona State University in 2005 and an MSEE degree from Southern Methodist University in 2009, respectively. He holds one U.S. patent on reducing power delivery AC noise in high speed IO interfaces.
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I. Introduction

In a typical computer system, multiphase DC-DC step-down buck converters are used to provide power to the processor core and cache, memory and other devices [1]. A simplified buck switching converter is shown in Figure 1. In the most commonly used PWM (pulse-width modulation) voltage regulator [2], the upper side and lower side FETs of each phase are switched on and off alternately to provide continuous current flow to the processor [2]. The processor loading often requires a fast rise/fall edge on FET gate voltage, where the edge rate could be as large as ~10-20V/ns. The high dv/dt and di/dt event associated with the fast gate voltage change and transient current flow during the FET on and off can be a major source of EMI. Studies of EMI problems due to VR have been published widely [3-6], while until recently, publications on Signal Integrity impacts of VR design are available [7-8].

![Figure 1: Simple buck switching voltage regulator](image)

It is not avoidable that critical signal lines (such as high speed differential busses, low-speed control lines, sense lines, clocks) will have to be routed in the proximity of the VR area due to the small form factors and lower cost designs. As a result, the VR switching event can generate significant amount of noise on the signals routed nearby. Careful VR layout is necessary to improve VR noise immunity and assure integrity of signals in proximity to the VR. In the past, most attention regarding to VR related signal integrity was focused on the spacing between the bus traces and VR FET components. Despite such care, many issues related to VR noise coupling into both high-speed and low-speed signals may still occur. These issues tend to be discovered late in the schedule and the impact to product cost and schedule can be very severe. Hence, it is critical to have a solid simulation methodology to discover potential noise coupling problems and explore mitigation techniques, especially in the early design stage.

This paper discusses our simulation-based analysis procedures, measurement validation of such and the lessons we have learned concerning VR noise coupling mechanisms that help us to improve our future designs. In Section II, we discuss some of the possible
noise coupling mechanisms. Both time domain and frequency domain simulation methods are carried out, and their advantages and disadvantages are discussed in Section III. Simulation and measurement data of a server VR noise study are reported in Section IV, including various techniques to mitigate noise. Lastly, in Section V, we demonstrate how to use the near field scanning technique to detect potential VR noise problems.

II. VR noise coupling mechanisms
We discussed a few possible VR noise coupling mechanisms in 2009 DesignCon paper [7]. That paper focused primarily on capacitive coupling, where the transient current in one VR area fill induces VR noise in adjacent area fills. The noise can be further coupled into adjacent power fills due to poor decoupling, and impacts any signals referenced to these fills. The example in Figure 2 shows the measurement waveforms caused by the VR noise capacitive coupling on one of our previous generation server board designs and led to blue screen or system lockup. The culprit was a system initialization signal called FSB_INIT. The signal was found to be picking up noise from an independent 12V power fill that was sandwiched in between two “FET node” fills of that VR and capacitive coupled the noise from (see Figures 3). This system lockup problem required hours to days to reproduce because it was sensitive to temperature and part selection, etc, which made debugging very time consuming. We spent 6 to 8 weeks and untold man-hours in finding the root cause. We added decoupling capacitors on the 12V power fill in the later versions of the designs, an adequate solution but more expensive than ideal.

Figure 2: VR noise coupling from P12V FET node to power fill to signal
More recently, we have experienced reduced signal margin and memory failures for several boards caused by a different VR noise coupling mechanism. The VR noise induced by current loop changes during a switching event can be coupled to the nearby signal vias through VR power vias, as shown in Figure 4. The current loop in red color is the VR noise source, while the current loop in green color is the victim loop. The impact of this inductive via-to-via coupling is quite significant and the noise can be coupled to signals several millimeters away in the absence of adequate shielding.

In one of our platforms, we experienced greater than 150mv of VR noise when the signal via is a connector via. The via size is physically large, and the loop area of the victim signal is big. Figure 5 shows the measured noise waveform, where the yellow and cyan curves are the waveforms measured at victim signal. The noise spikes caused by high di/dt occur during the phase switching on and off event.
We have also experienced system failures caused by this inductive coupling mechanism where the victim signals are low-speed control lines, sense lines, clocks, etc. The example shown below in Figure 6 was caused by inductive via-to-via coupling onto JTAG signal from a memory VR. JTAG signal is a low speed control signal associated with memory controller or CPU debug functionality and may make the system hang if it is malfunctioning. In this design, the input caps of the memory VR are placed at the bottom side of the board while the VR FETs are placed at the top layer of the board. High di/dt was generated in those 12V FET vias when FETs are switching off and on. As Figure 7 shows, the VR noise induced by current loop changes of the memory VR vias on these JTAG vias can reach more than 300 mV.
III. Simulation methodology

One of the most critical aspects to address VR noise on IO signals is the simulation capability. Hence we can predict IO signals impacted by the VR noise of server board designs in the early design stage. In this section, we detail both time domain and frequency domain analysis-based simulation methodologies, for which commercially available simulation tools are applied.

Frequency domain based simulation methodology

Typically at the early stage of design, it is preferred to use frequency domain solver to investigate noise coupling schemes for different ports from location to location. Simulated frequency domain coupling coefficients (S/Y/Z-parameters) tell us about critical coupling magnitude and the corresponding frequencies that may be due to design issues. With those early assessment data, engineers may be able to mitigate some or all of those high frequency coupling points and eventually remove all high noise coupling phenomena from VR switching to signaling. For example, from a frequency domain transfer impedance plot, one may be able to find out if it is applicable to use different frequency response decoupling capacitors to mitigate high coupling at a certain frequency. Alternatively, one may want to relocate decoupling capacitors to change transfer impedance in order to avoid high coupling over certain frequency ranges.

Another approach to reduce the transfer impedance is to disrupt the coupling path by adding shielding vias. Figure 8 is a demonstration of how shielding vias help to minimize the noise coupling from a VR. There are 3 coupling coefficient curves from the VR port
to the signal port. The first curve noted as ‘0’ indicates that there is no gnd via shielding in between a VR noisy via and a signal via. Curve nodes labeled as ‘4’ have 4 gnd vias isolated between VR noisy via to signal via and similarly for curve noted as ‘8’. One may see that with the 8 gnd via case, there is a lower coupling coefficient than is observed in the other 2 cases. Hence, adding gnd shielding vias is a useful method to mitigate noise coupling.

Figure 8: Coupling coefficient and shielding via relationship for mitigating VR noise coupling

After design optimization in frequency domain for all interested ports, it is a general practice to run transient simulations with assumed noise sources and receivers, so that we can have a more quantitative analysis of noise level. We need to obtain VR transistor models as noise generation sources, as well as electrical models of signal path as victims, to simulate noise coupling from switching VR to signals. Figure 9 lists the general flow of frequency approach.
However, there are a few technical challenges in order to have an accurate, well converged simulation to predict that noise. One of those challenges is how to use S parameters in transient analysis with adequate accuracy. There are a few approaches such as direct convolution or using the macro-modeling approach which actually converts S parameters into some a SPICE compatible subcircuit. Both approaches have advantages and disadvantages. Here, we apply the macro modeling approach for our convenience. Figure 10 demonstrates the basic simulation setup of running transient simulation based on frequency domain response for the system, augmented by circuit components for the VRs and signal drivers/receivers.
**Time domain based simulation methodology**

On the other hand, direct time domain system simulation can overcome the above challenges and can be directly compared to scope measurements. There are a few important learnings for running time domain simulations to analyze the VR noise issues [7].

First, the actual SPICE models of the VR devices are not always available and we have to generate behavioral models based on the data sheet as indicated in Figure 11. More details of the technique can be found in [7].

![Behavioral FET Model](image)

**Figure 11: Behavioral FET Model**

After we obtained the required FET models as well as the controller models, we verified the VR related circuit with a simple time domain tool, such as HSPICE. The main purpose is just to verify that the ideal VR circuit that behaves correctly but does not include all the coupling between planes, shapes or vias, etc.

We regularly perform this same type of time domain system simulation for various boards. To be more efficient with our engineering time, we automated the process for simulation setup. We developed a setup script to find all receivers, drivers, and resistive loads, for the important pins and attach simple but reasonable models with parasitics for them in the simulation system. We also pre-calculated the output inductor current and output capacitor voltage and applied those as initial conditions in the time domain simulation, in order to eliminate the lengthy simulation time required for VR settling.
Board layouts should to be close to completion, especially for the power fills and GND fills in order to accurately reflect the noise at the power planes and power vias in the simulation. However, power fills are usually the last to be completed and takes much longer time to simulate for a full board system in time domain. Therefore, we prefer to use time domain analysis for the late stage of designs to verify overall system performance. The general flow chart is shown below in Figure 12.

![Diagram](https://via.placeholder.com/150)

**Figure 12:** general flow about using time domain solver to predict noise coupling schemes from switching VR to signals

### IV. Simulation and measurement on a real case study

Simulations using both methods described above (frequency domain and time domain simulations) were performed for various VR designs on our server boards and correlated to lab measurements, including a memory VR case study shown in the following.

Figure 13 shows a two phase memory VR design denoted as PVDDQ. As shown in the figure, memory connectors are placed next to this VR, hence there are quite a few signal vias very close to 12V FET vias. Input decoupling capacitors of 12V FETs are placed at the bottom of the board. These 12V FET vias connect the 12V plane (on the top layer) to the decoupling capacitors on the bottom layer. During FET switching events, a high di/dt transient is induced from the bottom layer to the top layer through these 12V FET vias. The closeby signal vias, such as TP_46, can pick up a significant amount of noise due to coupling between connector vias and 12V FET vias. We applied both frequency domain and time domain methods for this analysis. The tools we chose were Sigrity PowerSI for frequency domain simulation and Sigrity Speed2000 for time domain simulation. In Figure 13, both PowerSI simulation and Speed2000 simulation are shown in a relative good agreement for the noise level picked up by TP_46 at the DIMM pin. We simulated 240mV pk-pk noise with PowerSI and simulated 207mV pk-pk noise with Speed2000. The slight difference may be caused by tool accuracy, model conversion issues (from frequency domain to time domain) and different initial condition setups in different simulators.
Figure 13: PVDDQ VR Layout

[Image: A circuit diagram showing PVDDQ VR layout with labels TP_46 at R1307, 12V FET fill, TP_46 DIMM pin, and annotations for Lots of 12V FET vias and Input caps.]

Figure 14: Simulation comparison for frequency domain (PSI/HSPICE) and for Time domain (Speed2k) at DIMM connector pin

[Graph showing PSI/HSPICE with a peak-to-peak value of 240mV and Speed2k with a peak-to-peak value of 207mV.]

Noise coupling to TP_.46 at DIMM pin

PSI/HSPICE

240mV Pk-Pk

Speed2k

207mV Pk-Pk
In addition, we compared the simulation with measurement for TP_46 at R1307, where the termination resistors are located. There is some attenuation of the noise due to the transmission line loss effects from the DIMM pin location to R1307. The noise for TP_46 at the R1307 is 90mV pk-pk (vs. 207mV pk-pk at the DIMM connector pin) from the simulation and is 98mV pk-pk from the measurement (see Figure 15). The small discrepancy may be caused by the scope noise floor, test point lead length, VR operating conditions, probe or scope settings.

![Noise coupling to TP_46 at R1307](image)

Figure 15: Noise coupling simulation (Speed2K) and measurement correlation for TP_46 at R1307

To mitigate the noise coupling, we moved the decoupling caps to the top layer, added the gnd shielding vias in between victim signal vias and 12V_FET vias, and change 12V FET planes to layer 5 instead of layer top (see Figure 16). We verified the changes in the time domain simulation as shown in Figure 17. The noise level for TP_46 at R1307 is decreased to less than 20mV pk-pk.
Figure 16: Layout changes: moved input capacitors to the top layer, changed 12V FET plane and added shielding vias

Figure 17: Simulation data for TP_46 after the layout changes
We also took the noise measurement on TP_46 on the new fabricated board with the above design changes. As you can see in Figure 18, the noise level is reduced to below 20mV pk-pk.

![Image](image_url)

**Figure 18**: Measurement data for TP_46 after the layout changes

V. Near Field Scanning

Due to the complexity of the design, it is desirable to have a brute force measurement-based technique to identify and verify potential noise sources. We chose near field scanning techniques [9-10] because a spatial distribution of the near field around VR routing area can be readily obtained through an automatic scanning procedure. Figure 19 shows the near field scanning results of a motherboard around DIMM memory design area. Only H field plots are shown herein since we care mostly about the di/dt event. The field plot was superimposed on the digital picture of the board using photo processing software for better illustration. Since VR components were mounted on top of board, while scanning was performed on bottom layer of the board, a hot spot in the picture means a di/dt transition occurred and it is very likely that transition penetrated the board and resulted in via-to-via noise coupling mechanism as shown in Figure 4.
The “hot spots” revealed by near field scanning corresponded very well to the switching noise source as described in previous discussion of coupling mechanisms. There are two similar VR designs in the same figure, on the top half and the bottom half of the picture. The bottom VR shows less noise, since in this particular case, we only drive 2/3 of the current as compared to the top VR. The metal pin columns on the left of Figure 17a and 17b correspond to the tails of the Dimm connector metal pins. Noise can be readily picked by connector pins in proximity to the hot spots. Interestingly, we also identified additional unanticipated VR noise sources. Our focus was mainly on the decoupling capacitors placed on bottom of the board, but the near field scanning results revealed that the snub filter circuit was a significant noise source as well. The reason we did not notice those additional noise sources is that we luckily did not have any critical signals routed in proximity to them. This finding reinforces the advantage of using near field scanning to identify potential VR noise sources.

VI. Summary
This paper discussed several VR coupling mechanisms and our methodology for finding the root cause of various VR coupling issues. We detailed both time domain and frequency domain analysis-based analysis methodologies. We discussed the design changes implemented through routing modification, adding shielding vias, etc, to disrupt the coupling path between the noise source and the victim signal. The effectiveness of
design changes were validated by both simulation and measurements. In addition, near field scanning measurement was performed and shown it is a brute force measurement-based technique to identify potential noise sources.